FIG 1 Section A-A (PRIOR ART)

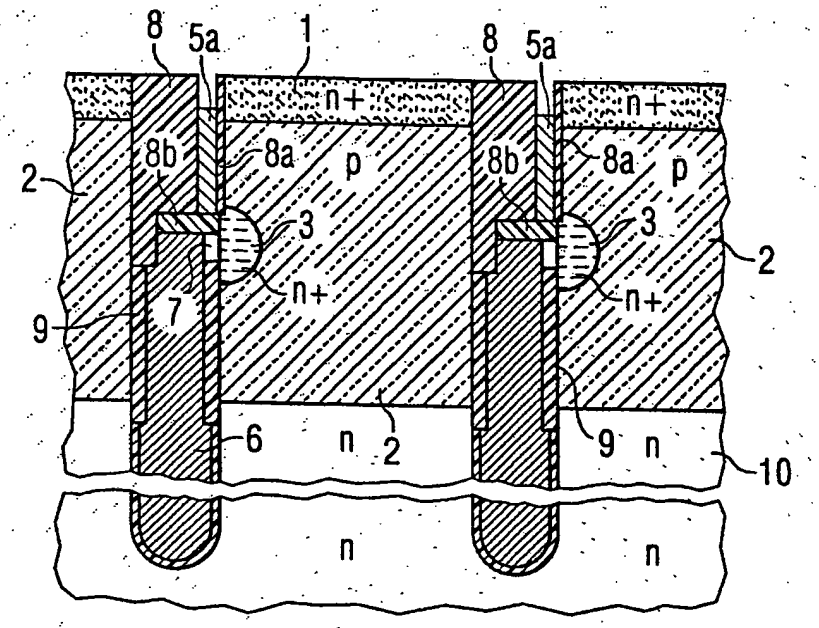
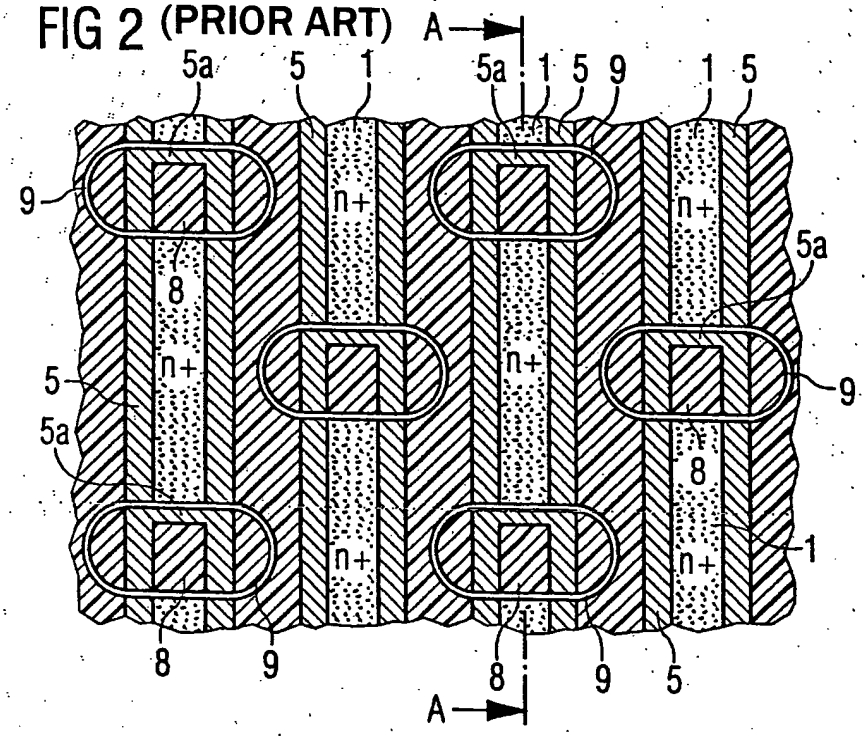


FIG 2 (PRIOR ART)



Gate

Webs (AT) (Source region)

p (channel area)

Poly Si/ tungsten/WL

Isolation/ dielectric

Drain region